REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-7 remain in the application. Claims 1, 3-4, and 6-7 have been amended.

In the section entitled "Claim Objections" on page 2 of the above-identified Office action, claims 3 and 6-7 have been objected to because of informalities. Appropriate correction has been made.

In item 1 on pages 2-3 of the above-mentioned Office action, claims 1-3 have been rejected as being anticipated by Park et al. (US Pat. No. 6,326,268) under 35 U.S.C. § 102(b).

In item 2 on pages 3-5 of the above-mentioned Office action, claims 4-7 have been rejected as being anticipated by Park et al. under 35 U.S.C. § 102(b).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references. However, the language of claims 1 and 4 has been

slightly modified in an effort to even more clearly define the invention of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> before the upper boundary layer is applied and after the application of the storage layer, applying a sacrificial layer made from polysilicon and a material selectively etchable with respect to a material of the storage layer to the storage layer;
>
> producing openings in the sacrificial layer, the storage layer, and the lower boundary layer, extending to the semiconductor body, by using a mask;
>
> introducing doped polysilicon into the openings;
>
> removing the sacrificial layer; and
>
> producing the upper boundary layer on the storage layer and oxidizing at least a proportion of the polysilicon to form the oxide region.

Claim 4 calls for, inter alia:

> before producing the upper boundary layer and after the application of the storage layer, applying a sacrificial layer with a topside to the storage layer;
>
> producing openings with lateral walls in the sacrificial layer, the storage layer, and the lower boundary layer, by using a mask;
>
> introducing dopant into implantation regions of the semiconductor body through the openings;
>
> etching back the lateral walls of the openings and a topside of the sacrificial layer at an etching rate

sufficient to form smooth sides on the sacrificial layer, the storage layer, and the lower boundary layer;

removing residues of the sacrificial layer selectively with respect to the storage layer; and

producing the upper boundary layer on the storage layer and forming an oxide region on a free surface of the semiconductor body, in each case between the sides.

Park et al. describe a method of fabricating a MONOS cell, in which an implantation of dopant is performed using a nitride layer with openings as a mask. Subsequently, the opening is filled with an oxide, which covers the doped region and is provided to form an electric insulation above the doped region. The detailed description of Fig. 3 in column 3 designates the first applied layer 36 as a pad silicon oxide layer and the second applied layer 38 as a silicon nitride layer to be utilized in a later CMP process. Fig. 3 shows the implantation of the doped region including regions 26 and 28. According to the second paragraph in column 4, the opening is overfilled with silicon oxide 42. The surface is planarized down to the upper surface of the silicon nitride layer 38. Then, both the silicon nitride layer 38 and the pad silicon oxide layer 36 are removed as shown in Fig. 6 as described in column 4, lines 37-40. After the pad silicon oxide layer 36 has been removed, the ONO structure 30 is grown to overlie the semiconductor substrate.

Contrary to the Examiner's statement in the Office action, the silicon oxide layer 36 does not form the lower boundary layer of the charge-trapping memory layer sequence. The nitride layer 38 can be regarded as some kind of sacrificial layer, which helps to perform method steps and is later removed. However, the layer 38 is not applied upon the sequence of the lower boundary layer and the storage layer, before the upper boundary layer is applied.

In contrast, the inventive method according to the invention of the instant application makes use of a sacrificial layer (10) that is applied on the storage layer (4). The doped region and the electric insulation formed by an oxide layer above the doped region are either produced by the application of doped polysilicon, which is subsequently oxidized, or by an implantation according to the prior art with a subsequent widening of the applied layer sequence so that a larger area of the semiconductor surface can be oxidized, as shown in Fig. 9 of the instant application. The oxidation takes place after the sacrificial layer has been removed. Therefore, the sequence of method steps according to the invention of the instant application by which the storage layer is applied, the sacrificial layer is deposited, openings are formed by lithography in the regions provided for the bitlines, a formation of doped regions takes place either by an

implantation of doping atoms or by the out-diffusion of dopant from an applied polysilicon layer, the sacrificial layer is removed, and the oxidation is performed either by an oxidation of the semiconductor body after the opening has been enlarged or by an oxidation of the applied polysilicon, is substantially different from the sequence of method steps disclosed by Park et al. In Park et al., firstly, the implantation takes place, secondly, the oxide is deposited, thirdly, the semiconductor surface is laid bare, and fourthly, the memory layer sequence is applied as an NONO layer sequence. The order of method steps in the method described in Park et al. is therefore reversed as compared to the method steps in the method of the invention of the instant application. This is clearly recited in the claims of the instant application, which include the limitations that the sacrificial layer is removed before the upper boundary layer and the insulation above the doped region are produced by an oxidation step.

Park et al. do not disclose filling doped polysilicon into the openings of the layer sequence of the lower boundary layer, the storage layer, and the sacrificial layer, nor do Park et al. disclose the method by which the lateral walls of the openings are etched back to form smooth sides as shown in Fig. 8 of the instant application. The only etching step after the

application of the bit-line oxide region 22 in the method of Park et al. is performed to remove the layers 36 and 38 completely from the semiconductor surface without maintaining any residual layer parts. In the method of Park et al., there is no sacrificial layer, storage layer, and lower layer to form the smooth sides or sidewalls since the storage layer is applied only after the complete removal of the layers 36 and 38.

It is accordingly believed to be clear that Park et al. do not show or suggest the features of claims 1 and 4. Claims 1 and 4 are, therefore, believed to be patentable over Park et al. and since all of the dependent claims are dependent on claims 1 or 4, they are believed to be patentable as well.

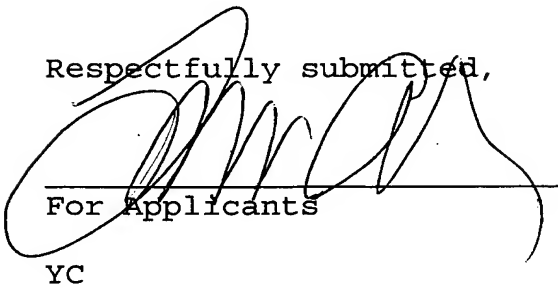
In view of the foregoing, reconsideration and allowance of claims 1-7 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to

the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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